IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent application of	:	
Young-Goo Lee	:	Group Art Unit 2822
Serial No. 10/029,147	:	Examiner Maria F. Guerrero
Filed December 28, 2001	:	

METHOD OF FABRICATING SEMICONDUCTOR DEVICE FOR PREVENTING CONTAMINATING PARTICLE GENERATION

REQUEST FOR RECONSIDERATION AFTER FINAL

U.S. Patent and Trademark Office
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Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

Sir:

This is in response to the final Office action dated October 21, 2003.

35 U.S.C. ¶102 and ¶103

Claims 1-12 were rejected under 35 U.S.C. ¶103 as being unpatentable over Nakano et al. (US 6534384) in view of Jones et al. (US 6117778) and/or Liu et al. (US 6287961). Applicants respectfully traverse this rejection.

Nakano et al. is directed to the formation of a silicon-on-insulator (SOI) substrate by adhering two wafers 1 and 2 to one another and then subjecting the adhered wafers to the processes illustrated in FIGS. 1(a) – (j) thereof. These steps are summarized below:

FIG.1(b): Upper wafer 1 having insulating layer 3 is adhered to lower wafer 2;

FIG. 1(c): Oxidation is carried out, resulting in insulating layer 4;

FIG. 1(d): Side portions of upper wafer 1 are grinded;

FIG. 1(e): Remaining side portions of upper wafer 1 are etched away;

FIG. 1(f): Upper wafer 1 (1') is subjected to polishing;

FIG. 1(g): Upper wafer 1 (1") is subjected to PACE;

FIG. 1(h): Masking tape 6 is placed on upper wafer 1"; and

FIGS. 1(i)-(j): Peripheral etching is carried out.

FIG. 2A of Nakano et al. corresponds to the results obtained after the polishing process of FIG. 1(f) of Nakano et al. Specifically, the upper silicon wafer 1' is polished at FIG. 1(f), whereby, as shown in FIG. 2A, the insulating layer (buried oxide 5) remains between the upper and lower silicon wafers. In other words, the upper silicon wafer 1' is polished, but the underlying oxide layer 5 is not polished. Nakano et al. does not teach polishing the oxide layer 5 as apparently suggested by the Examiner.

Further, the present claims recite coating of a photoresist on the planarized layer having the uniform and non-uniform regions. In contrast, Nakano et al. teaches the placement of a masking tape 6 on the silicon layer 1".

Nakano et al. does not teach depositing a layer to a predetermined thickness on a wafer, and then planarizing the deposited layer to remove a portion of the deposited layer, where the resulting planarized layer includes a uniform region of uniform

thickness extending along a wafer surface, and a non-uniform region of non-uniform thickness corresponding to an upper sidewall of the wafer. That is, mentioned above, Nakano et al. polishes the upper silicon wafer 1'.

Further, Nakano et al. does not teach coating a photoresist layer on the planarized layer. Rather, Nakano et al. teaches the placement of a masking tape 6 on the silicon layer 1" (i.e., the portion of the wafer 1' remaining after PACE).

As a separate matter, it is noted that the present invention is generally directed to minimizing the thickness of a deposited layer remaining at a dead zone region of the wafer. In contrast, Nakano et al. is generally directed to bonding/adhering of a thin layer by planarization and heat-treatment processes.

For at least the reasons stated above, Applicants respectfully contend that claims 1-12 are neither anticipated by, nor rendered obvious in view of, the teachings of the cited references, taken individually or in combination.

Conclusion

No other issues remaining, reconsideration and favorable action upon the claims 1-12 now present in the application are requested.

Respectfully submitted,

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